REMARKS

I. Introduction

In response to the pending Office Action, Applicants have amended claim 4 so as to address the rejection of claims 4, 8 and 9 under 35 U.S.C. § 112, second paragraph. Claim 3 has been amended to further clarify the intended subject matter of the invention. Claim 10 has been cancelled. No new matter has been added.

Applicants respectfully traverse the rejection of claims 2-5 and 8-10 under 35 U.S.C. § 112, first paragraph, for the reasons set forth below.

II. The Rejection Of Claims 2, 3, 5 And 10 Under 35 USC § 112, First Paragraph

Claims 2, 3, 5 and 10 were rejected under 35 U.S.C. § 112, first paragraph. It is asserted in the pending rejection that the recitation in claims 2 and 3 regarding that the comparator functions to compare an edge of the clock signal, on which the data signal is intended to be latched, to one of a leading edge and a trailing edge of the data signal during each cycle of the clock signal, is unsupported in the original specification. Applicants respectfully disagree.

The Examiner's attention is directed to, for example, page 18, line 23 to page 19, line 13, wherein the specification expressly states that while the present invention can operate in a mode in which the comparator compares the clock signal with both the leading and trailing edges of the data signal, the present invention can also operate in a

mode in which the comparator compares the clock signal with only the leading edge of a data signal, or in a mode in which the comparator compares the clock signal with only the trailing edge of a data signal. In other words, another possible mode of operation is to only compensate for the delays associated with a low-to-high data transition (adjusted by delay circuit 31) or delays associated with a high-to-low data transition (adjusted by delay circuit 32). As such, the generation of both control signals Cde1F/B and Cde2F/B is not always necessary.

Thus, it is respectfully submitted that the claim language objected to under 35 U.S.C. § 112, first paragraph, is clearly supported in the original specification, and therefore it is requested that the rejection be withdrawn.

III. The Rejection Of Claims 4, 8 And 9 Under 35 USC § 112, Second Paragraph

Claims 4, 8 and 9 were rejected under 35 U.S.C. § 112, second paragraph. In response to this rejection, Applicants have amended claim 4 so as to clarify that the first and second delay circuits do not make their respective comparisons utilizing the same edge of the clock signal. As amended, the claim makes clear that the first delay circuit and second delay circuit utilize a first edge and a second edge of the clock signal, respectively when performing their respective operation. It is submitted that the amendment to claim 4 overcomes the pending rejection.

IV. The Rejection Of Claims 3 And 10 Under 35 USC § 102

Claims 3 and 10 were rejected under 35 U.S.C. § 102 as being anticipated by USP No. 6,178,212 to Akashi. Applicants respectfully submit that, as amended, claim 3 is patentable over Akashi for at least the following reasons.

As amended, claim 3 recites in pertinent part, a "delay means defines the first delay time based on the result of a first comparison between the clock signal and the leading edge of the data signal and the second delay time based on the result of a second comparison between the clock signal and the trailing of the data signal performed by the comparator"

One exemplary embodiment of the "delay means" of the present invention is shown in Fig. 1 of the specification, wherein, for example, delay section 60 outputs the T2 + T1 (setup time) delayed clock signal CLK2 when the data D1 transits from low to high and/or outputs the T3 + T1 (setup time) delayed clock signal CLK2 when the data D1 transits from high to low.

In the pending rejection, element 20 of Akashi is asserted as corresponding to the claimed "delay means." However, in contrast to the delay means of the present invention, element 20 merely control the amount of delay according to an intermediate phase set by the intermediate phase setting means 24, which calculates an intermediate phase between the rising edge and falling edge of the input data Din. In other words, element 20 provides the same amount of delay time regardless whether

the data transits from low to high or from high to low. Akashi does not disclose or suggest generating a first delay time associated with a data transition from low to high and a second delay time associated with a data transition from high to low. Thus, at a minimum, Akashi fails to disclose or suggest the foregoing element recited by amended claim 3.

Accordingly, as anticipation under 35 U.S.C. § 102 requires that ***each element of the claim*** in issue be found, either expressly described or under principles of inherency, in a single prior art reference, ***Kalman v. Kimberly-Clark Corp.***, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983), for the foregoing reasons, it is clear that Akashi does not anticipate claim 3, or any claim dependent thereon.

V. All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, ***Hartness International Inc. v. Simplimatic Engineering Co.***, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 3 and 4 are patentable for the reasons set forth above, it is respectfully submitted that all pending dependent claims are also in condition for allowance.

VI. Request For Notice Of Allowance

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

McDERMOTT, WILL & EMERY

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